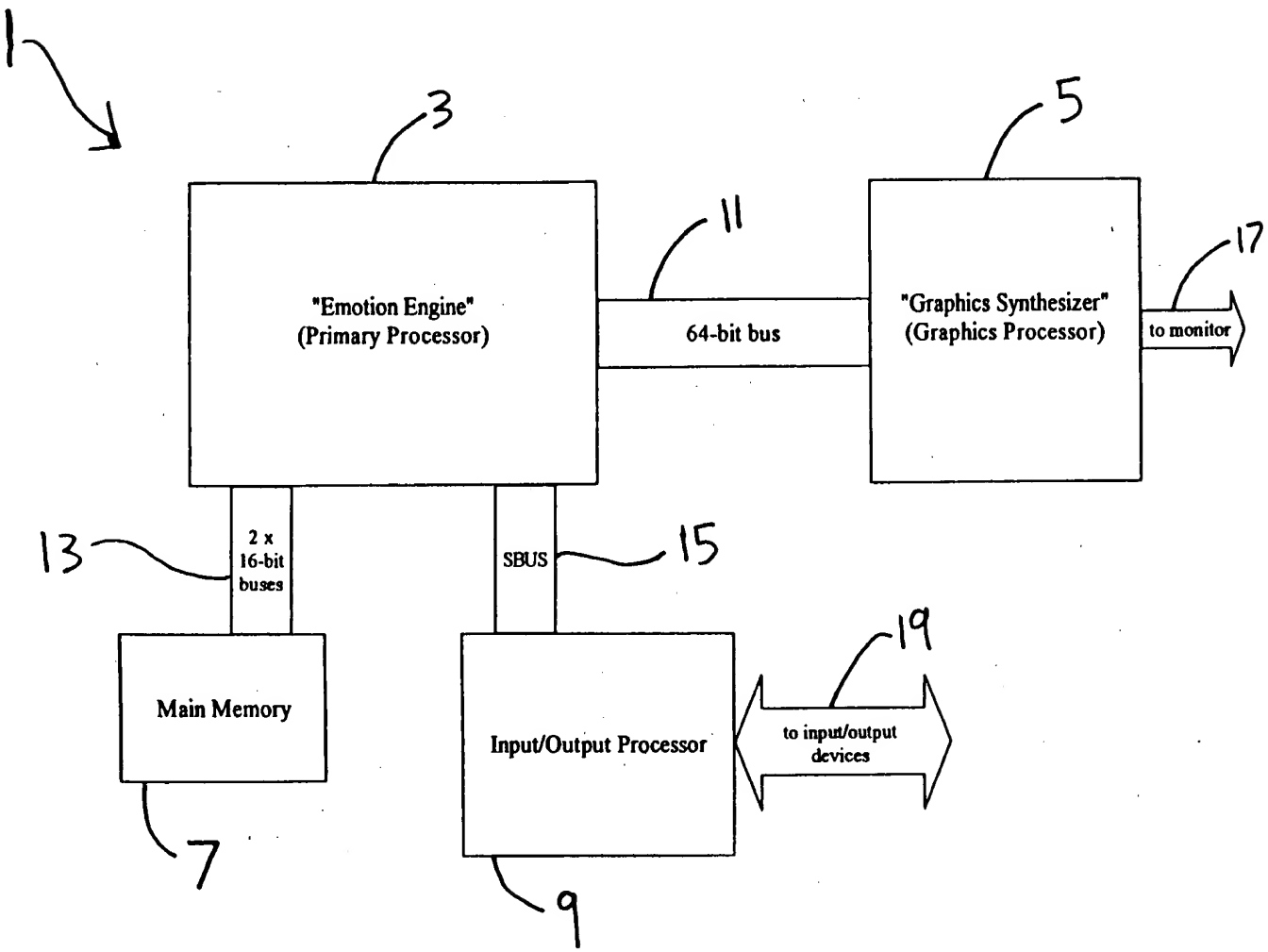

Fig. 1

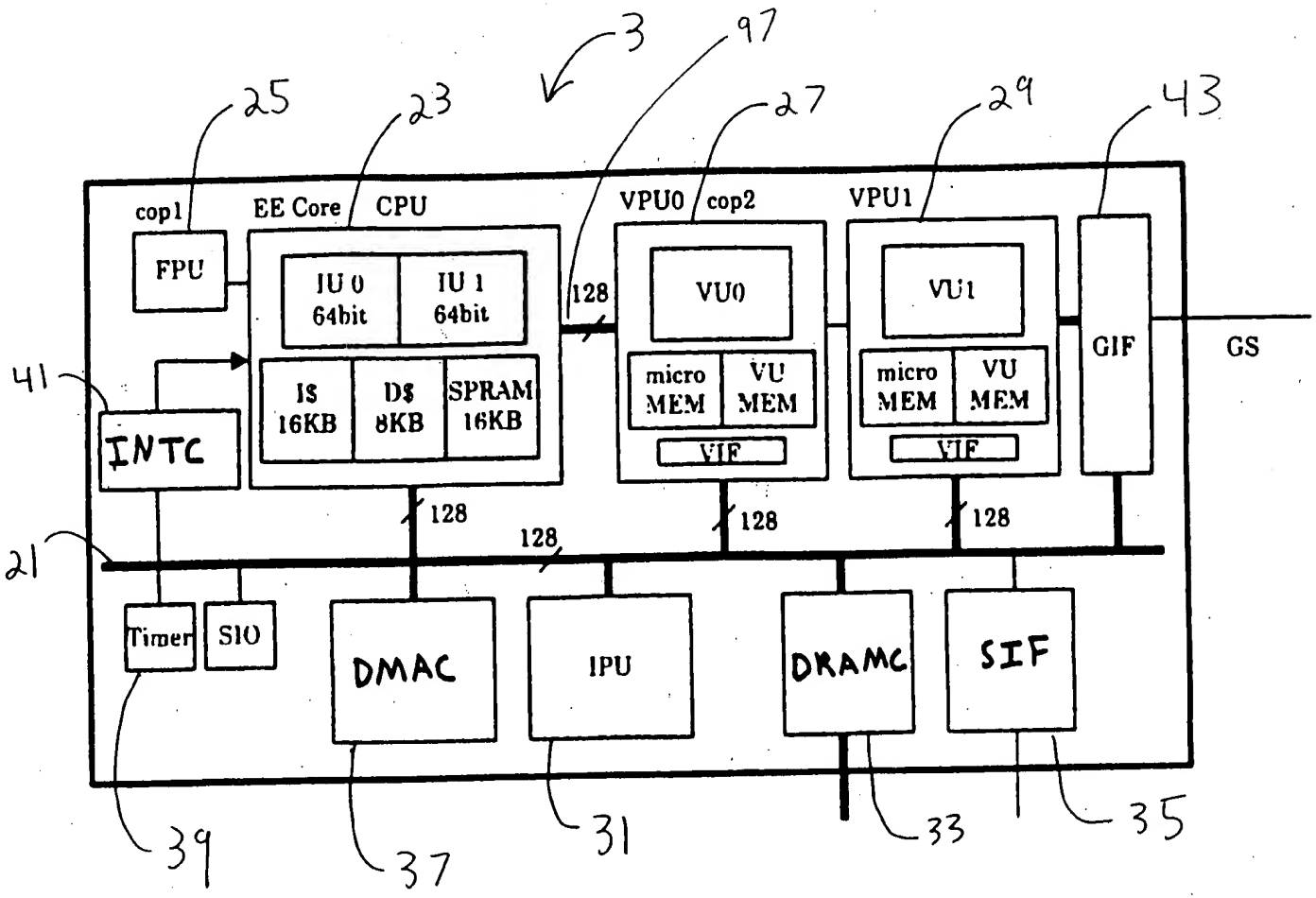

Fig. 2

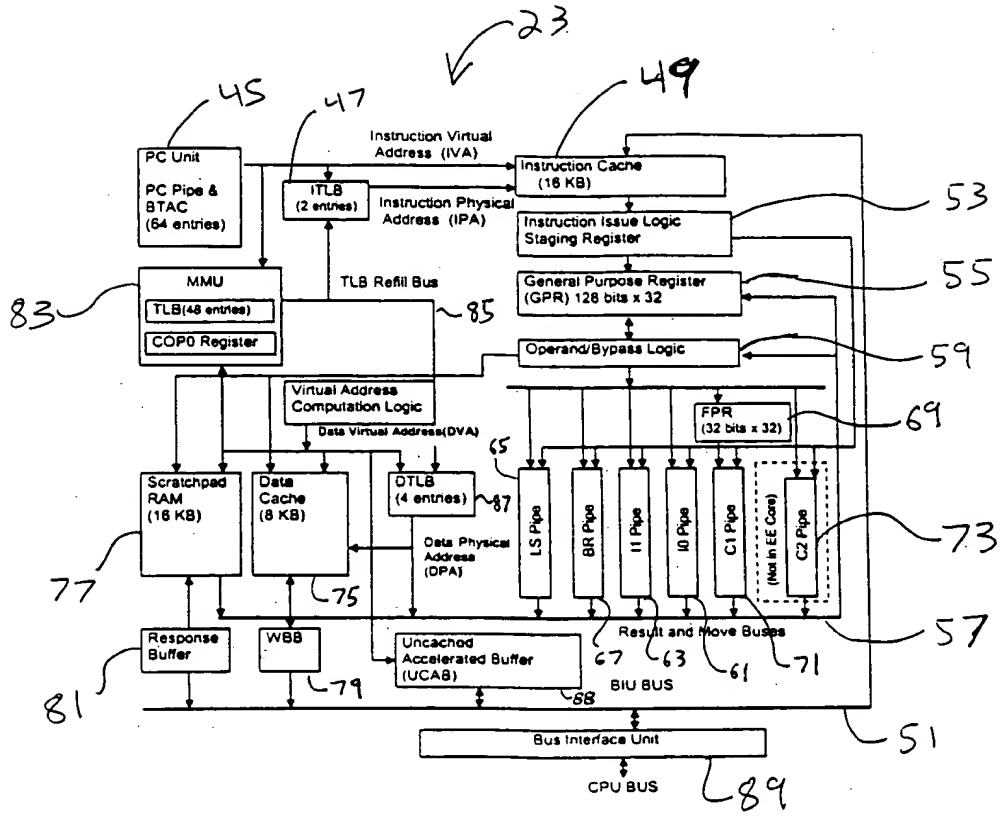
23
45
47
49
PC Unit
PC Pipe & BTAC (64 entries)
ITLB (2 entries)
Instruction Virtual Address (IVA)
Instruction Physical Address (IPA)
Instruction Cache (16 KB)
Instruction Issue Logic Staging Register
53
General Purpose Register (GPR) 128 bits x 32
55
Operand/Bypass Logic
59
MMU
TLB(48 entries)
COP0 Register
83
TLB Refill Bus
85
Virtual Address Computation Logic
Data Virtual Address(DVA)
FPR (32 bits x 32)
69
65
Scratchpad RAM (16 KB)
Data Cache (8 KB)
DTLB (4 entries)
87
LS Pipe
BR Pipe
I1 Pipe
I0 Pipe
C1 Pipe
(Not in EE Core)
C2 Pipe
73
Data Physical Address (DPA)
77
75
Response Buffer
WBB
Uncached Accelerated Buffer (UCAB)
Result and Move Buses
67
63
61
71
57
81
79
88
BIU BUS
Bus Interface Unit
51
CPU BUS
89

Fig. 3

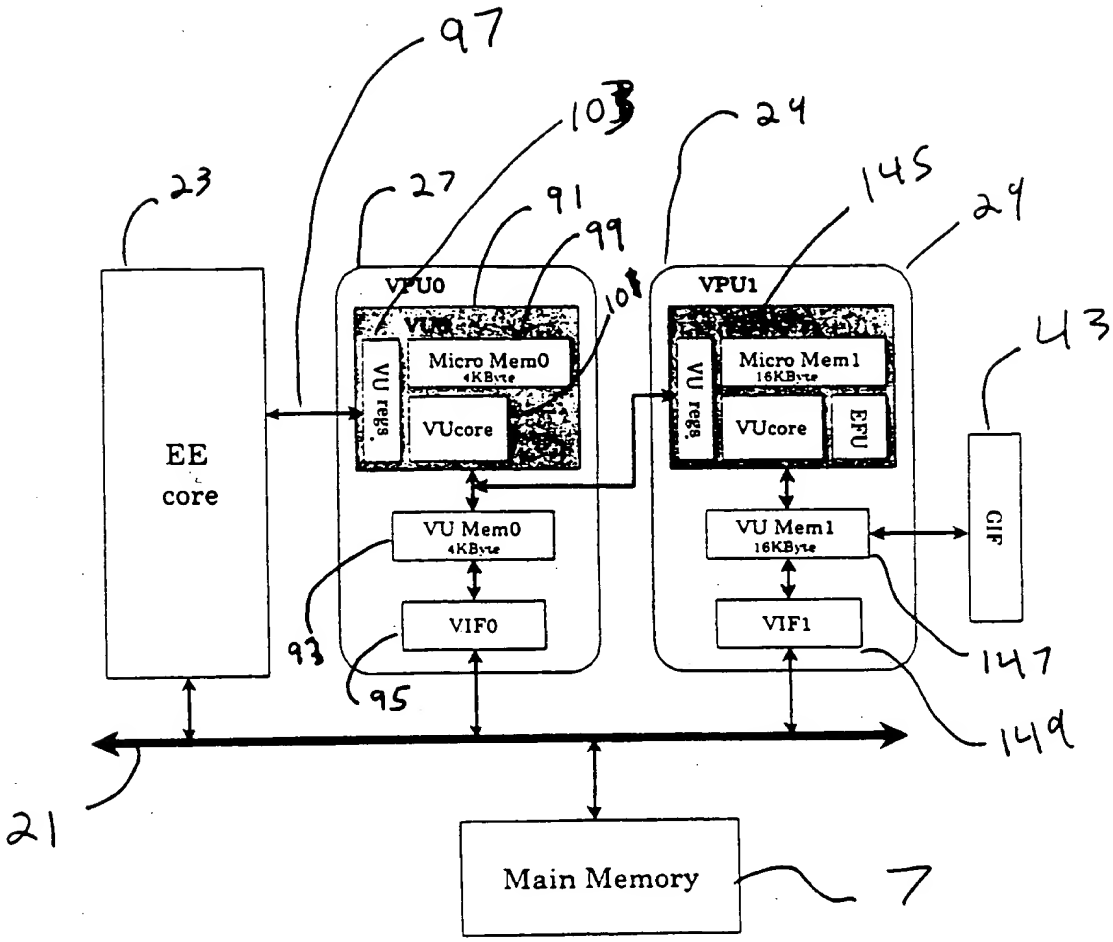
97
103
24
23
27
91
145
29
99
VPU0
VPU1
101
43
Micro Mem0
4KByte
Micro Mem1
16KByte
VU regs
VUcore
EFU
EE
core
GIF
VU Mem0
4KByte
VU Mem1
16KByte
VIF0
VIF1
93
95
147
149
21
Main Memory
7

Fig. 4

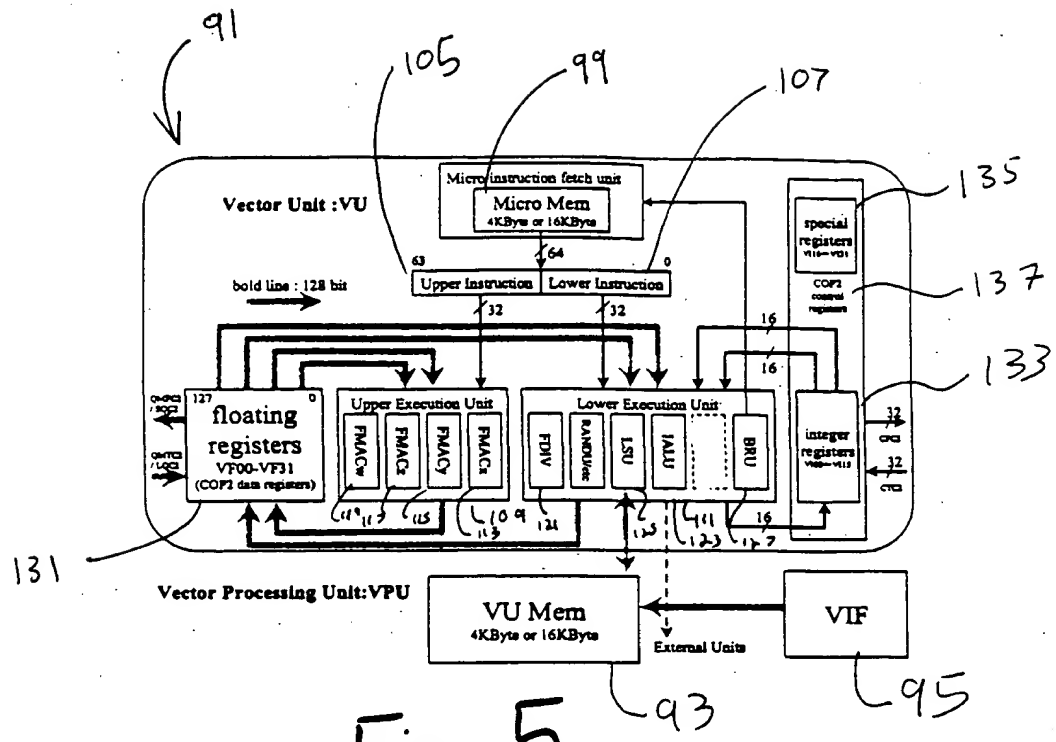
91
105
99
107
135
137
133
131
Vector Unit :VU
Micro instruction fetch unit
Micro Mem
4KByte or 16KByte
bold line : 128 bit
Upper Instruction
Lower Instruction
63
64
0
32
32
16
16
special registers
COP2 control registers
floating registers
VF00-VF31
(COP2 data registers)
127
0
Upper Execution Unit
FMACw
FMACx
FMACy
FMACz
Lower Execution Unit
FDIV
RANDUnit
LSU
IALU
BRU
integer registers
32
32
Vector Processing Unit:VPU
VU Mem
4KByte or 16KByte
External Units
VIF
93
95

Fig. 5

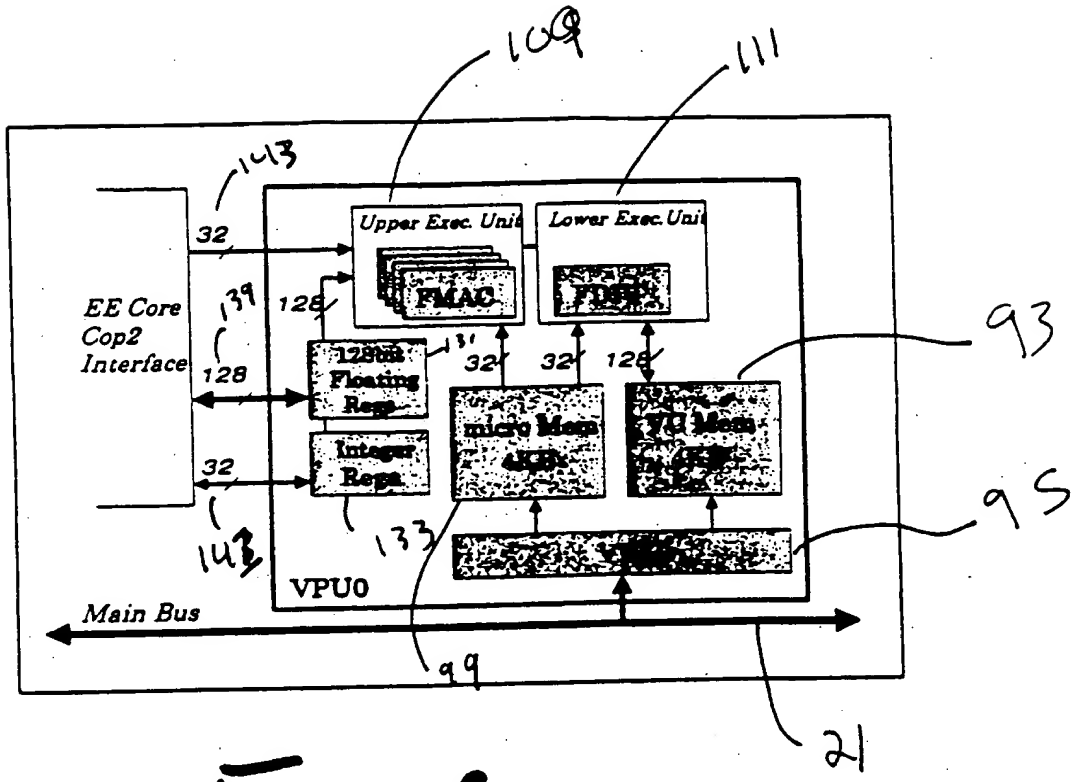
109
111
143
32
Upper Exec. Unit
Lower Exec. Unit
FMAC
EE Core
Cop2
Interface
139
128
128
32
32
128
93
Floating
Reg.
Integer
Reg.
micro Mem
VU Mem
32
143
133
95
VPU0
Main Bus
99
21

Fig. 6

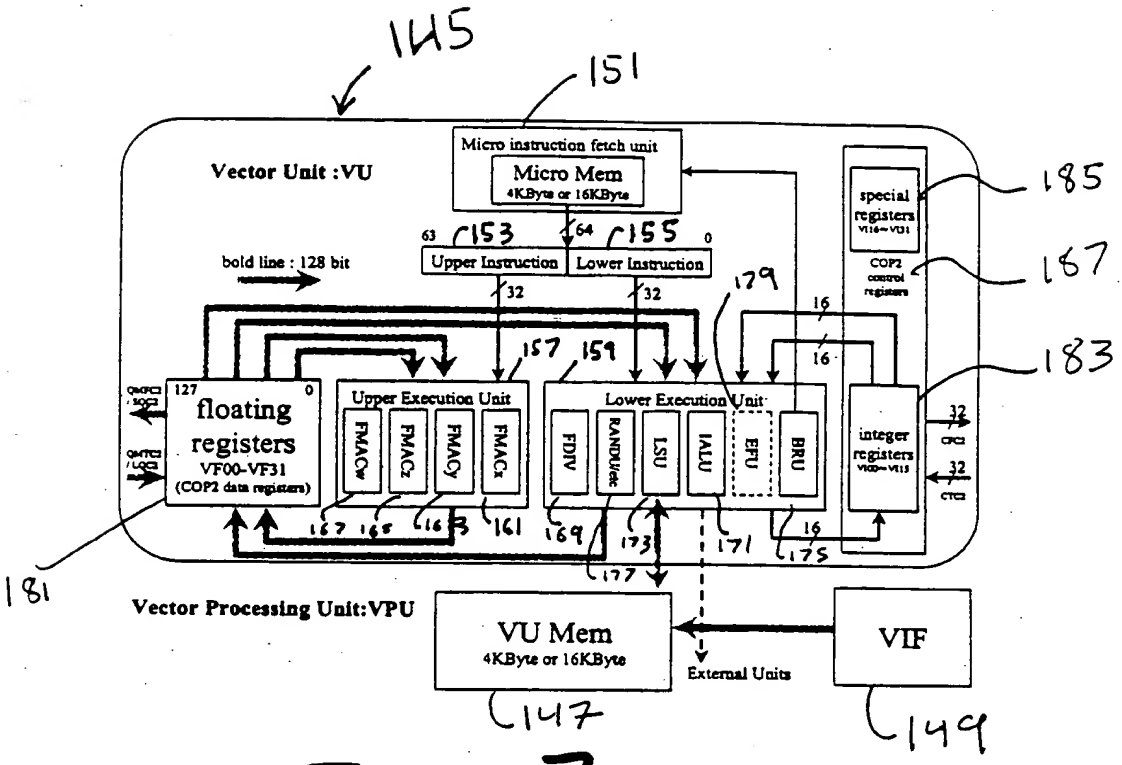
145
151
Vector Unit :VU
Micro instruction fetch unit
Micro Mem
4KByte or 16KByte
bold line : 128 bit
63
153
64
155
0
Upper Instruction
Lower Instruction
32
32
179
16
16
special registers
185
COP2 control registers
187
183
157
159
127
0
floating registers
VF00-VF31
(COP2 data registers)
Upper Execution Unit
FMACw
FMACz
FMACy
FMACx
Lower Execution Unit
FDIV
RANDU/ERANU
LSU
IALU
EFU
BRU
integer registers
VI00~VI15
32
32
167
165
163
161
169
173
171
175
177
181
Vector Processing Unit:VPU
VU Mem
4KByte or 16KByte
External Units
VIF
147
149

Fig. 7

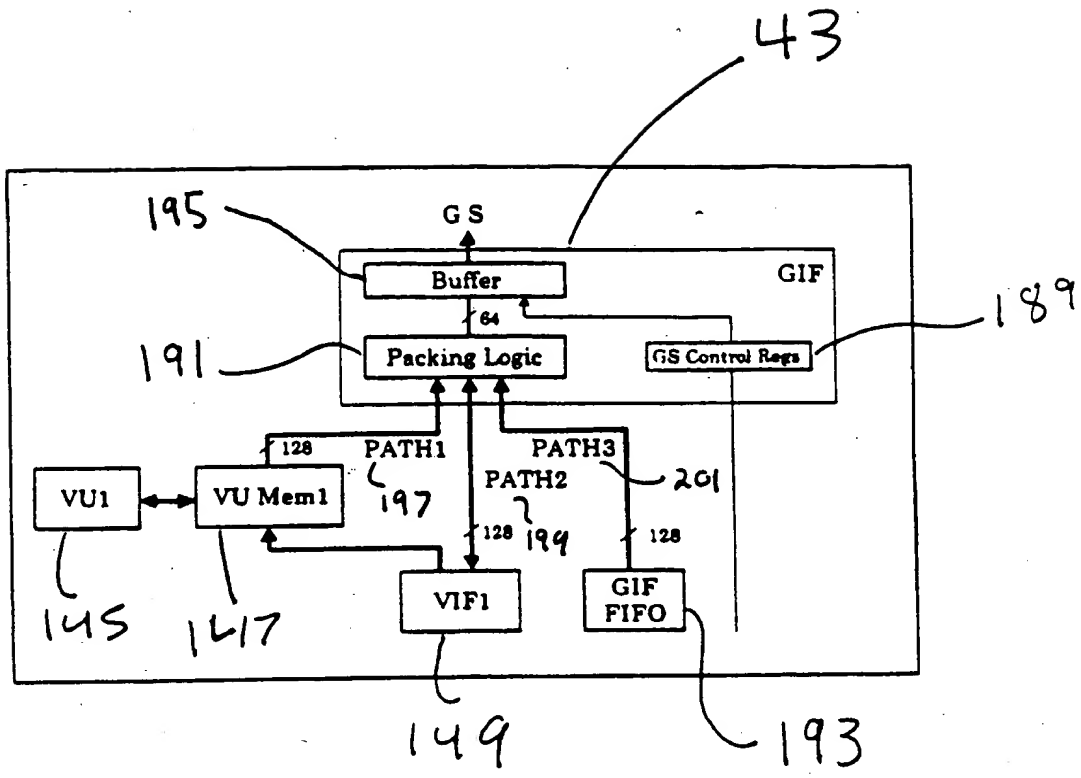
43
195
GS
Buffer
GIF
64
189
191
Packing Logic
GS Control Regs
128
PATH1
PATH3
PATH2
201
VU1
VU Mem1
197
128
199
128
VIF1
GIF
FIFO
145
147
149
193

Fig. 8

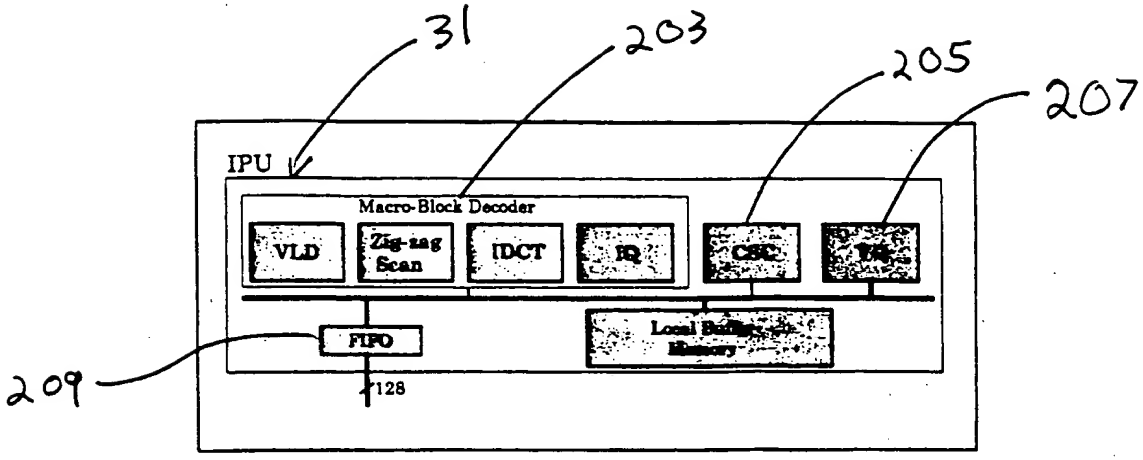
31
203
205
207
IPU
Macro-Block Decoder
VLD
Zig-zag Scan
IDCT
IQ
CSC
FIFO
128
209

Fig. 9

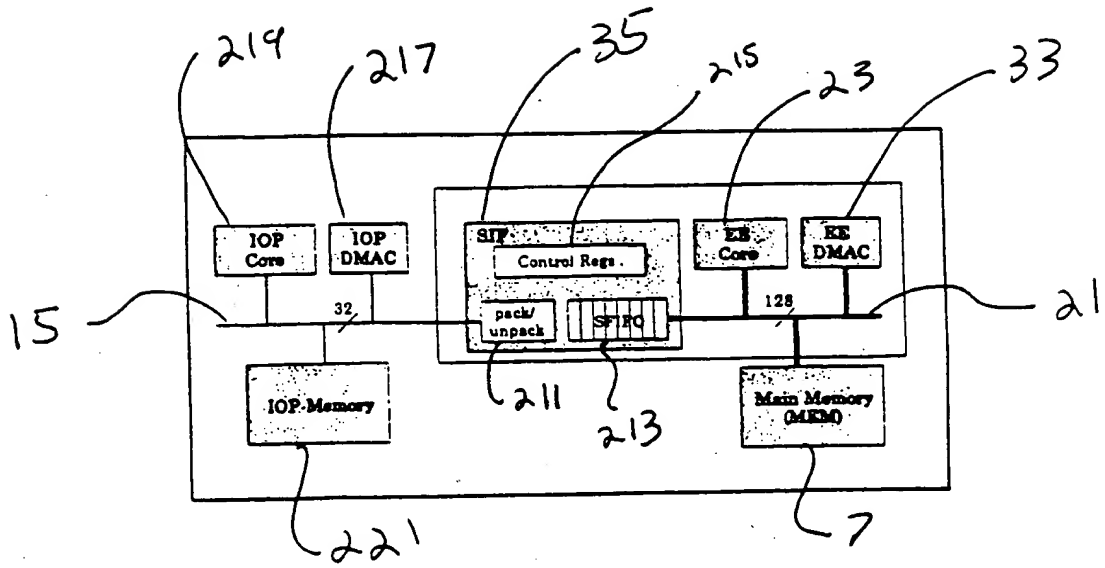
219
217
35
215
23
33
IOP Core
IOP DMAC
SIF
Control Regs.
pack/ unpack
SFIFO
EE Core
EE DMAC
32
128
15
21
IOP Memory
Main Memory (MEM)
211
213
221
7

Fig. 10

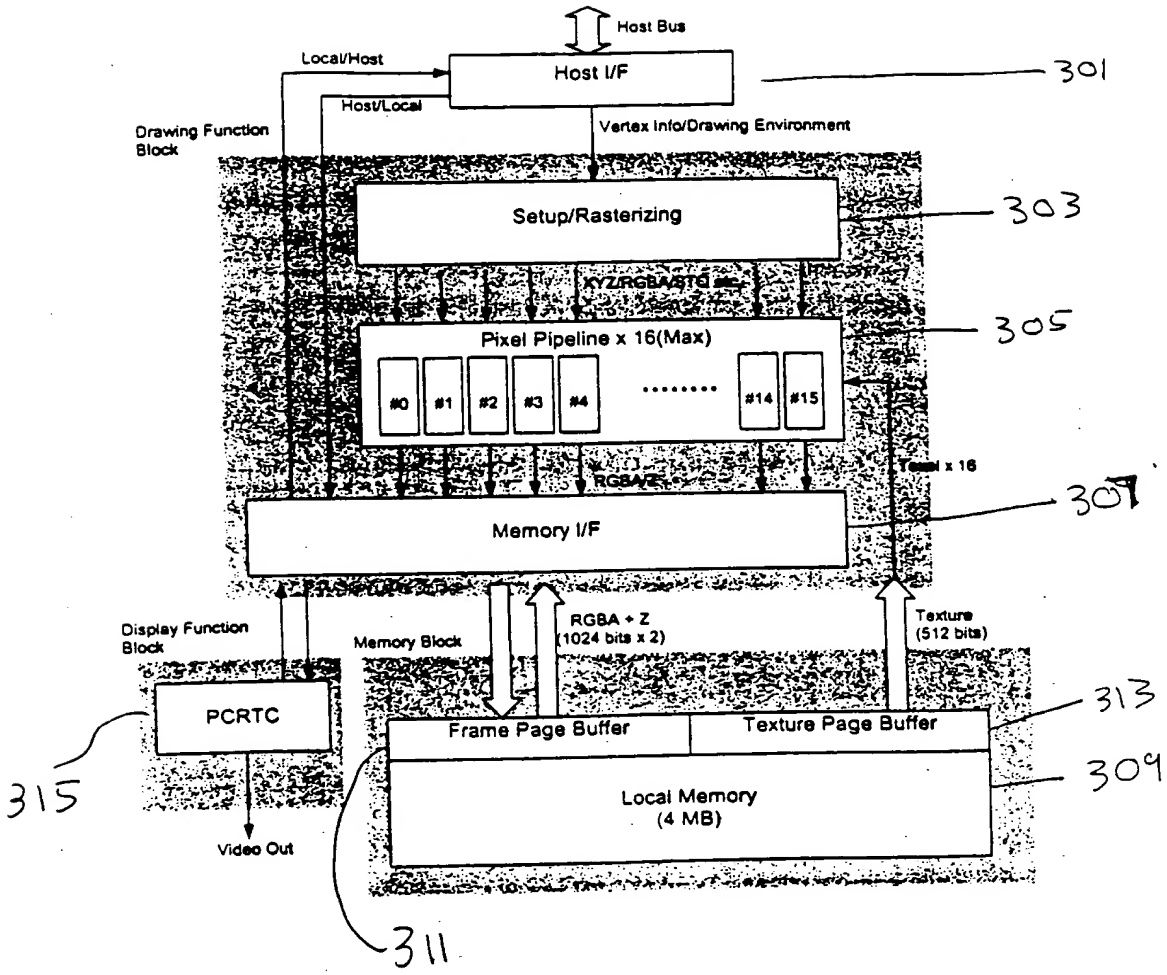
Host Bus
Local/Host
Host I/F
301
Host/Local
Drawing Function Block
Vertex Info/Drawing Environment
Setup/Rasterizing
303
XYZ/RGBA/STQ
Pixel Pipeline x 16(Max)
305
#0
#1
#2
#3
#4
#14
#15
RGBA/Z
Texel x 16
307
Memory I/F
Display Function Block
Memory Block
RGBA + Z (1024 bits x 2)
Texture (512 bits)
PCRTC
313
Frame Page Buffer
Texture Page Buffer
309
Local Memory (4 MB)
315
Video Out
311

Fig. 11

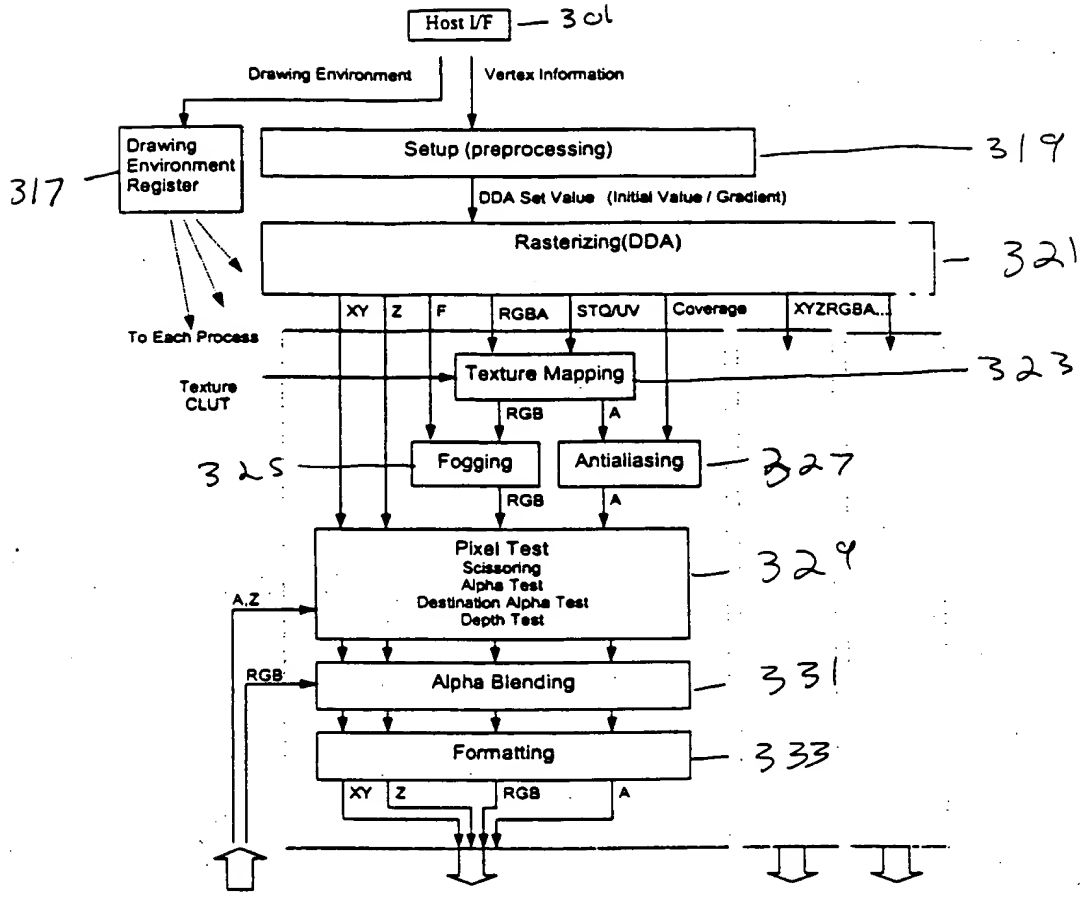
Host I/F
301
Drawing Environment
Vertex Information
Drawing Environment Register
317
Setup (preprocessing)
319
DDA Set Value (Initial Value / Gradient)
Rasterizing(DDA)
321
XY
Z
F
RGBA
STQ/UV
Coverage
XYZRGBA...
To Each Process
Texture Mapping
323
Texture CLUT
RGB
A
325
Fogging
Antialiasing
327
Pixel Test
Scissoring
Alpha Test
Destination Alpha Test
Depth Test
329
A,Z
RGB
Alpha Blending
331
Formatting
333

Fig. 12

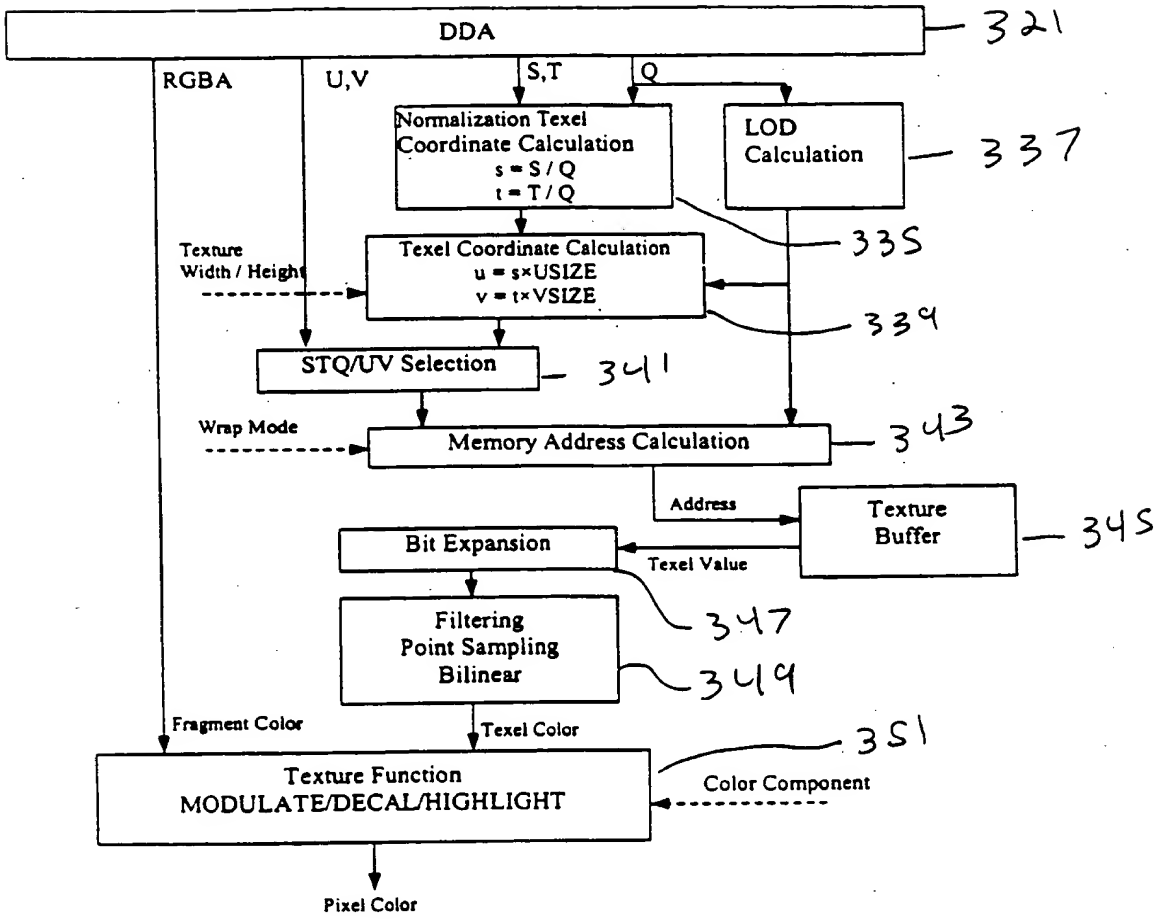
DDA
321
RGBA
U,V
S,T
Q
Normalization Texel Coordinate Calculation
s = S / Q
t = T / Q
LOD Calculation
337
335
Texture Width / Height
Texel Coordinate Calculation
u = s×USIZE
v = t×VSIZE
339
STQ/UV Selection
341
Wrap Mode
Memory Address Calculation
343
Address
Texture Buffer
345
Bit Expansion
Texel Value
347
Filtering
Point Sampling
Bilinear
349
Fragment Color
Texel Color
351
Texture Function
MODULATE/DECAL/HIGHLIGHT
Color Component
Pixel Color

Fig. 13